Modeling of High Voltage Devices for ESD Event Simulation in SPICE

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Outline

- **INTRODUCTION**
  - ESD & general ESD protection scheme
  - Background of SPICE ESD simulation for HV devices

- **HV LDMOS DEVICES AND ESD PROTECTION**
  - High voltage NLDMOS devices
  - HV ESD protection clamp

- **SNAPBACK MODELING**
  - Operation of LDMOS and HV clamp
  - Snapback models for LDMOS and HV clamp

- **MEASUREMENT AND SIMULATION**

- **CONCLUSION**
Introduction
-- What is ESD?

◆ ESD: Electrostatic Discharge
Sudden electrostatic charge transfer between two objects at different potentials

◆ Causes:
Tribo-electric charging and electrical field induction

◆ In ICs:
Occurs in human handling and testing

◆ Characteristics:
  ● Large currents and high voltages
  ● Short in duration (1~150 ns)
Why focus on ESD?

- **ESD causes damages in ICs**
  - Catastrophic failures: contact spiking, junction burnout, gate oxide rupture, metal burnout
  - Latent failures: degradation of gate oxide, partial opens in metals

- **Costly failure mechanism**
  - Costs electronics industry >$84B in lost profits per year (4~8% of total annual revenue!)*
  - Responsible to >30% customer returns

(* M. Brandt & S. Halperin, *Circuits Assembly Magazine*, June 1, 2003)
Objective: protect IC from ESD damages
1. Shunt current discharges away from the CORE CIRCUIT
2. Clamps I/O & Power pad voltage to a safe level

Interaction of ESD protection and core circuitry
- Ideally, ESD structures are transparent to internal circuitry
- In reality, the protection and core circuitries impact each other’s performance
Motivation of SPICE ESD simulation for HV Devices

- BCDMOS technology is key in mixed-signal applications for multiple sectors
- Co-design is required for robust ESD protection design and circuit optimization in high voltage mixed-signal applications
- Circuit-level simulation provides useful insight in the interaction between ESD protection and core circuitry
- Simulation can reduce design iteration and cost that typically occur in trial-and-error approaches
SPICE ESD Simulation for HV Devices Co-Design Conditions

HV Device Between Two I/O Pads

Control Circuit

I/O_1

I/O_2

ger

n-p-n

Body

HV Device HV Protection Clamp Co-design

Control Circuit

VG

VH'

R_{IO}

VL

HV Clamp

WCM 2011, June 15-16, Boston
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A key requirement for ESD simulation is the availability of compact models accurate for ESD operation.

ESD modeling for HV devices is very challenging:
- Devices operate in extreme bias conditions
- Structure complexity of LDMOS and HV clamps

There are very few reported modeling efforts which are either not self-consistent or have limited availability.

SPICE simulation using macromodel approach has been demonstrated successful in low voltage technologies.

Similar modeling approach for HV LDMOS devices and HV clamps will be presented in this paper.
LDMOS DEVICES AND ESD PROTECTION
-- High Voltage NLDMOS devices

- Non-uniform channel doping
- Lightly doped N-Well/Deep N-Well drift region
Operation of LDMOS

- High voltage LDMOS devices can snapback under ESD stress condition due to turn-on of parasitic BJT
- There is a significant current increase before the device snapbacks to a lower voltage
Operation of LDMOS (cont.)

- The BJT does not turn-on until the applied voltage is significantly higher than the breakdown voltage of the Drain/Bulk junction
  - The breakdown starts in the depletion zone of the N-Well to P-Well junction
  - The device snapbacks when the depletion region expands reaching the highly doped N+ Drain region
- $V_{t1}$ is significantly higher than regular MOS devices (20~120V vs. 5~10V)
- The snapback trigger voltage ($V_{t1}$) is less dependent to the rise time of stress pulses (such as TLP pulses)
- Highly sensitive to ESD-induced damage
Key Components and Effects in LDMOS Snapback

- **Key components**: main LDMOS, parasitic BJT, back-gate resistance, P-well/N-well diode
- **Key effects**: avalanche current at Drain/Back-gate (Collector/Base) junction, voltage drop across the back-gate resistance, P-well/N-well diode breakdown
Macro Model for LDMOS Snapback

- The main LDMOS MOS modeled by MOS20
- A NPN modeled with Mextram is for the parasitic BJT
- A resistor Rbg for the back-gate resistance
- A diode for the P-well/N-well junction
- Intrinsically includes all major effects in snapback

\[
I_d = I_d' + I_c
\]

\[
I_{ds} = I_{sub} - I_b
\]
LDMOS DEVICES AND ESD PROTECTION
-- ESD protection clamp

- A thyristor-type (SCR) device with bi-directional path for ESD discharge current
- The device can be decoupled into two separate bipolar transistors, a PNP and a NPN
Operation of HV Clamp

- The clamp works in snapback mode as a result of the positive feedback triggered by the avalanche current in the PNP and NPN
- In snapback, one BJT activates first and then subsequently the second one turns on
- The Vt1 is more determined by the first BJT while the second one has bigger impact on Vh
- The weaker the second BJT is, the higher the Vh
- Used as protection for LDMOS at I/O or as power clamp
- High Vt1 and sometimes high Vh are required for HV clamping
Macro Model for Thyristor-like Clamp

- The model includes the NPN, PNP, avalanche effect, and resistive voltage drop Vbe in the both BJT’s
- The clamp is modeled by incorporating an advanced BJT (NPN) model with two resistors
- $R_{pw} = 1\,\text{M}\Omega$ for floating Pwell
- The NPN model includes both the avalanche and junction capacitance and has a parasitic PNP that is used for the Qpnp
Transmission Line Pulse (TLP) Measurement Setup Introduction

- Experimental data were measured with TLP technique
- Apply a sequence of rectangular pulses to two terminals of a DUT
- Use stabilized I-V curves as measurement results

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Simulation Setup for Snapback Effect

- Snapback effect was simulated with transient simulation
- Voltage Pulse Sequence (100ns) were used as the Input
- The stabilized $V_D$ and $I_D$ were measured as the simulation results (~80ns).
Simulation Results vs. TLP Measurement

-- NLDMOS device (W=5000um, t_{rise}=10ns)
Simulation Results vs. TLP Measurement
-- NLDMOS device (W=200um) for different rise times
Simulation Results vs. TLP Measurement

-- NLDMOS device (W=200um) with longer drift region
Simulation Results vs. TLP Measurement
-- a low holding voltage clamp in the 0.35um process ($t_{\text{rise}}=10\text{ns}$)
Simulation Results vs. TLP Measurement

-- a high holding voltage clamp in the 0.18um process
Modeling ESD behavior of high voltage LDMOS and thyristor-like clamp devices using a macro model approach has been presented.

The models consisted of standard passive and active components without having to use a complex external dependent current source.

The simplicity of this modeling approach facilitates easy implementation of the methodology.

The simulation results have shown good agreement with measured TLP data as performed on 0.18-um and 0.35-um BCDMOS process technologies.
Acknowledgement

- **Slavica Malobabic**: For contributions on devices’ characterization, TCAD simulation and insightful discussion on the results presented in this paper.
- **Srivatsan Parthasarathy**: For valuable inputs on the development of this work.