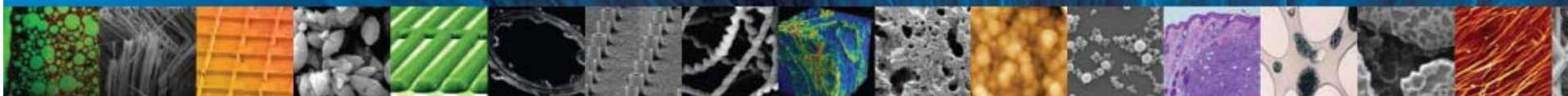




# Nanotech

Conference & Expo 2010



## Workshop on Compact Modeling

*Chair: Xing Zhou*



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# Workshop on Compact Modeling

## Wednesday June 23 (Morning)

- 8:30 Theory of Bipolar MOSFET (BiFET) with Electrically Short Channels
- 9:00 Impact of Gate-Induced-Drain-Leakage current modeling on circuit simulations in 45nm SOI technology and beyond
- 9:20 Modeling of Gate Leakage, Floating Body Effect, and History Effect in 32nm HKMG PD-SOI CMOS
- 9:40 A Unified Charge-Based Model for SOI MOSFETs Valid from Intrinsic to Heavily Doped Channel
- 10:00 *Break*
- 10:30 Non-Charge-Sheet Analytic Model for Ideal Retrograde Doping MOSFETs
- 10:50 Subthreshold Quantum Ballistic Current and Quantum Threshold Voltage Modeling for Nanoscale FinFET
- 11:10 Electrostatic Potential Compact Model for Symmetric and Asymmetric Lightly Doped DG-MOSFET Devices
- 11:30 Analytic Channel Potential Solution of Symmetric DG AMOSFETs
- 11:50 Source/Drain Edge Modeling for DG MOSFET Compact Model
- 12:10 *Lunch*

# Workshop on Compact Modeling

## Wednesday June 23 (Afternoon)

- 1:30 Xsim: Benchmark Tests for the Unified DG/GAA MOSFET Compact Model
- 1:50 Analytical Modeling of the Subthreshold Electrostatics of Nanoscale GAA Square Gate MOSFETs
- 2:10 A Continuous Compact Model of Short-Channel Effects for Undoped Cylindrical Gate-All-Around MOSFETs
- 2:30 Analytical Solution of Surface Potential for Un-Doped Surrounding-Gate MOSFET
- 2:50 Analytical model of quantum threshold voltage in short-channel nanowire MOSFET including band structure effects
- 3:10 *Break*
- 3:30 Bias Dependence of Low Frequency Noise in 90nm CMOS
- 3:50 Modeling of Mismatch and Across-Chip Variations in Compact Device Models
- 4:10 Improved Compact Model of Quantum Sub-band Energy Levels for MOSFET Device Application
- 4:30 Compact Modeling of Signal Transients for Dispersionless Interconnects With Resistive, Capacitive and Inductive Terminal Loads
- 4:50 Guidelines for Verilog-A Compact Model Coding
- 5:10 *End*

# WCM: SOI/Bulk Models

8:30 am – 10:00 am. Session Chair: Xing Zhou, Singapore

- **Theory of Bipolar MOSFET (BiFET) with Electrically Short Channels (*invited*)**  
*B.B. Jie, C-T. Sah, University of Florida, US*
- **Impact of Gate-Induced-Drain-Leakage current modeling on circuit simulations in 45nm SOI technology and beyond**  
*H. Wang, R. Williams, L. Wagner, J. Johnson, P. Hyde, S. Springer, IBM, US*
- **Modeling of Gate Leakage, Floating Body Effect, and History Effect in 32nm HKMG PD-SOI CMOS**  
*Y. Deng, R.A. Rupani, J. Johnson, S. Springer, IBM, US*
- **A Unified Charge-Based Model for SOI MOSFETs Valid from Intrinsic to Heavily Doped Channel**  
*J. Zhang, J. He, L. Zhang, X. Zhou, Z. Zhou, Peking University, CN*

# WCM: DG MOSFET Models

10:30 am – 12:10 pm. Session Chair: Bin Jie, USA

- **Non-Charge-Sheet Analytic Model for Ideal Retrograde Doping MOSFETs**  
*Z. Zhou, J. Zhang, X. Zhou, X. Lin, J. He, Peking University, CN*
- **Subthreshold Quantum Ballistic Current and Quantum Threshold Voltage Modeling for Nanoscale FinFET**  
*U. Monga, T.A. Fjeldly, UniK/Norwegian University of Science and Technology, NO*
- **Electrostatic Potential Compact Model for Symmetric and Asymmetric Lightly Doped DG-MOSFET Devices**  
*H. Abebe, E. Cumberbatch, S. Uno, V. Tyree, University of Southern California/ISI, US*
- **Analytic Channel Potential Solution of Symmetric DG AMOSFETs**  
*L. Chen, Y. Xu, L. Zhang, X. Zhou, W. Zhou, J. He, Peking University, CN*
- **Source/Drain Edge Modeling for DG MOSFET Compact Model**  
*T. Nakagawa, S. O'uchi, T. Sekigawa, T. Tsutsumi, M. Hioki, H. Koike, AIST (National Institute of Advanced Industrial Science and Technology), JP*

# WCM: GAA MOSFET Models

1:30 pm – 3:10 pm. Session Chair: Ning Lu, US

- **Xsim: Benchmark Tests for the Unified DG/GAA MOSFET Compact Model**

X. Zhou, G.J. Zhu, M.K. Srikanth, S.H. Lin, Z.H. Chen, J.B. Zhang, C.Q. Wei, Y.F. Yan, R. Selvakumar, Zhihuan Wang, *Nanyang Technological University, SG*

- **Analytical Modeling of the Subthreshold Electrostatics of Nanoscale GAA Square Gate MOSFETs**

S.K. Vishvakarma, U. Monga, T.A. Fjeldly, *Norwegian University of Science and Technology, NO*

- **A Continuous Compact Model of Short-Channel Effects for Undoped Cylindrical Gate-All-Around MOSFETs**

B. Cousin, M. Reyboz, O. Rozeau, M.-A. Jaud, T. Ernst, J. Jomaah, *CEA, LETI, MINATEC, FR*

- **Analytical Solution of Surface Potential for Un-Doped Surrounding-Gate MOSFET**

A. Dey, A. DasGupta, *Arizona State University, US*

- **Analytical model of quantum threshold voltage in short-channel nanowire MOSFET including band structure effects**

J. Dura, S. Martinie, D. Munteanu, M.-A. Jaud, S. Barraud, J.L. Autran, *CEA-LETI Minatec, FR*

# WCM: RF/Statistical/Atomic/Interconnect Models

3:30 pm – 5:10 pm. Session Chair: Xing Zhou, Singapore

- **Bias Dependence of Low Frequency Noise in 90nm CMOS**  
N. Mavredakis, A. Antonopoulos, M. Bucher, *Technical University of Crete, GR*
- **Modeling of Mismatch and Across-Chip Variations in Compact Device Models**  
N. Lu, *IBM, US*
- **Improved Compact Model of Quantum Sub-band Energy Levels for MOSFET Device Application**  
W. Feldman, E. Cumberbatch, H. Abebe, *University of Southern California/ISI, US*
- **Compact Modeling of Signal Transients for Dispersionless Interconnects With Resistive, Capacitive and Inductive Terminal Loads**  
Chi Liu, Z. Zhou, X. Lin, J. Xia, X. Zhang, J. He, *Peking University, CN*
- **Guidelines for Verilog-A Compact Model Coding**  
G. Depeyrot, F. Pouillet, *dolphin integration, FR*

## WCM 2011 – the 10<sup>th</sup> Anniversary

- All participants are welcome to join the Microsystem Focused Networking Reception (Room 303c) at 5:30pm
- Call for voluntary contribution of the presentation slides on Nanotech web
- Thank you all for your participation and look forward to seeing you at the 10<sup>th</sup> anniversary of WCM in Boston on June 13-16, 2011!