



Systems and Technology Group

Modeling of Gate Leakage, Floating Body Effect, and History Effect in 32nm HKMG PD-SOI CMOS

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IBM Microelectronics

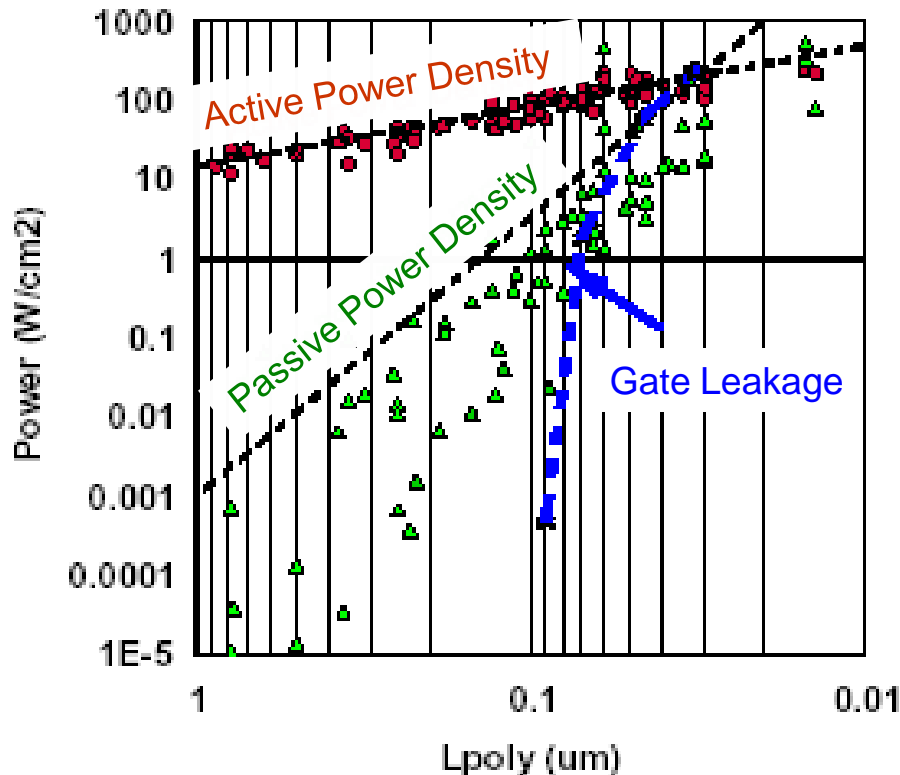
June 23, 2010

Outline

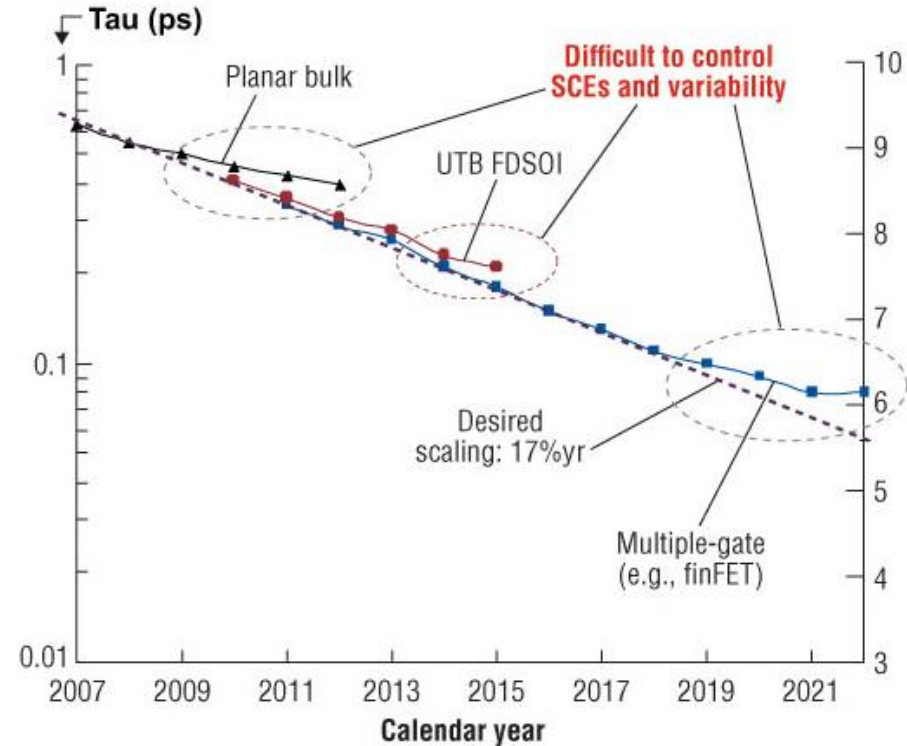
- ▣ **Introduction and Motivation**
- ▣ **Gate Leakage Modeling Procedures**
- ▣ **Modeling of Gate-to-body and Diode Currents**
- ▣ **Floating Body Effect and History Effect**
- ▣ **Modeling of Gate Leakage in 32nm HKMG PD-SOI CMOS**
- ▣ **Summary**

High-Performance Transistor Scaling

Scaling of Conventional Poly Gate Transistor [1]



Future Transistor Scaling [2]
($\tau = C \cdot V / I$)

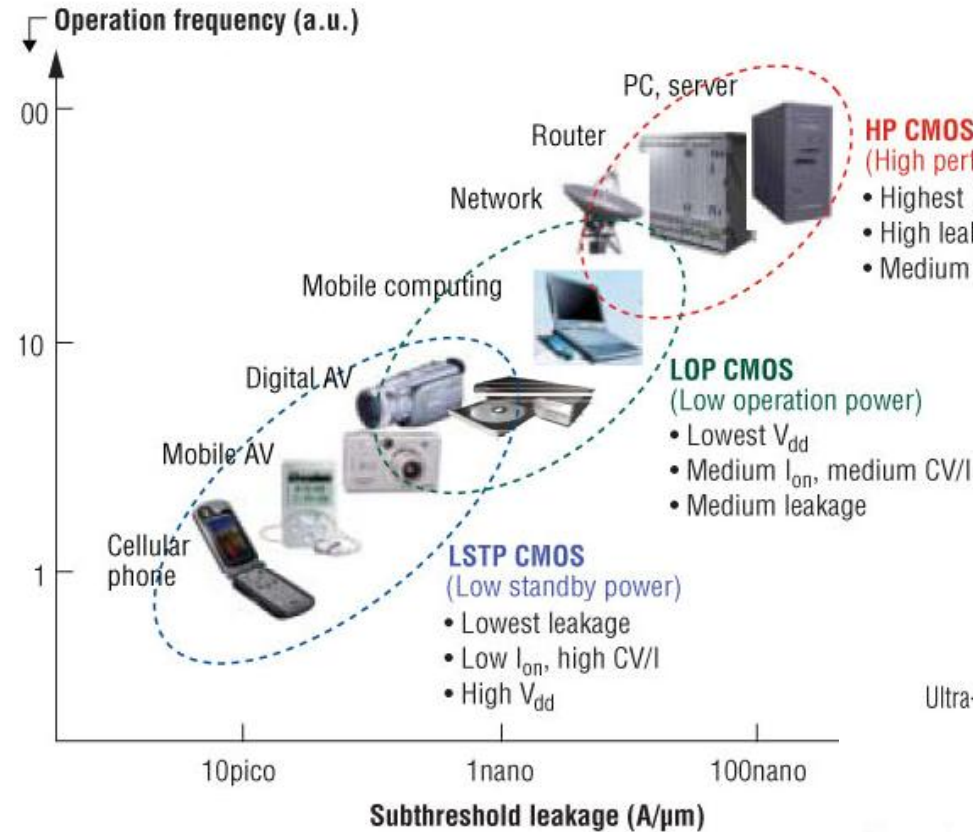


High-K Metal Gate Technology to Reduce Gate Leakage.

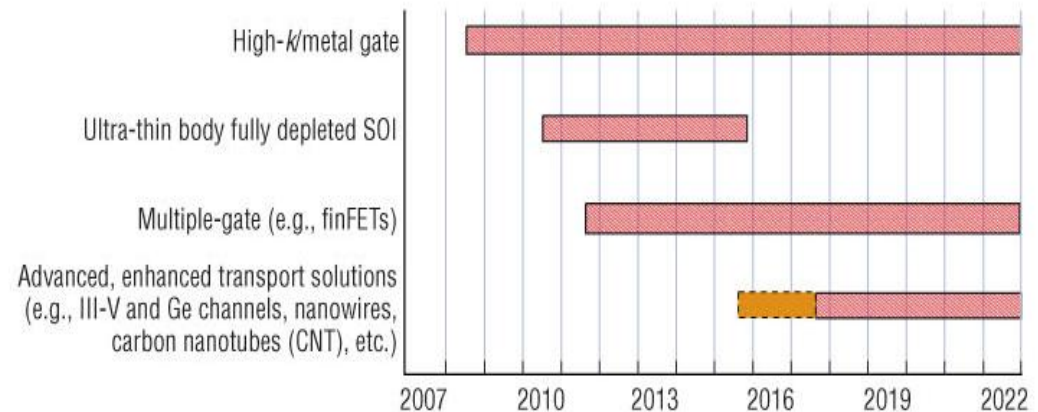
[1] Ching-Te Chuang, et al., p. 11, IEEE Circuit & Devices, Jan/Feb, 2004

[2] P. M. Zeitzoff, SST, p. 35, Feb, 2008

Subthreshold Leakage

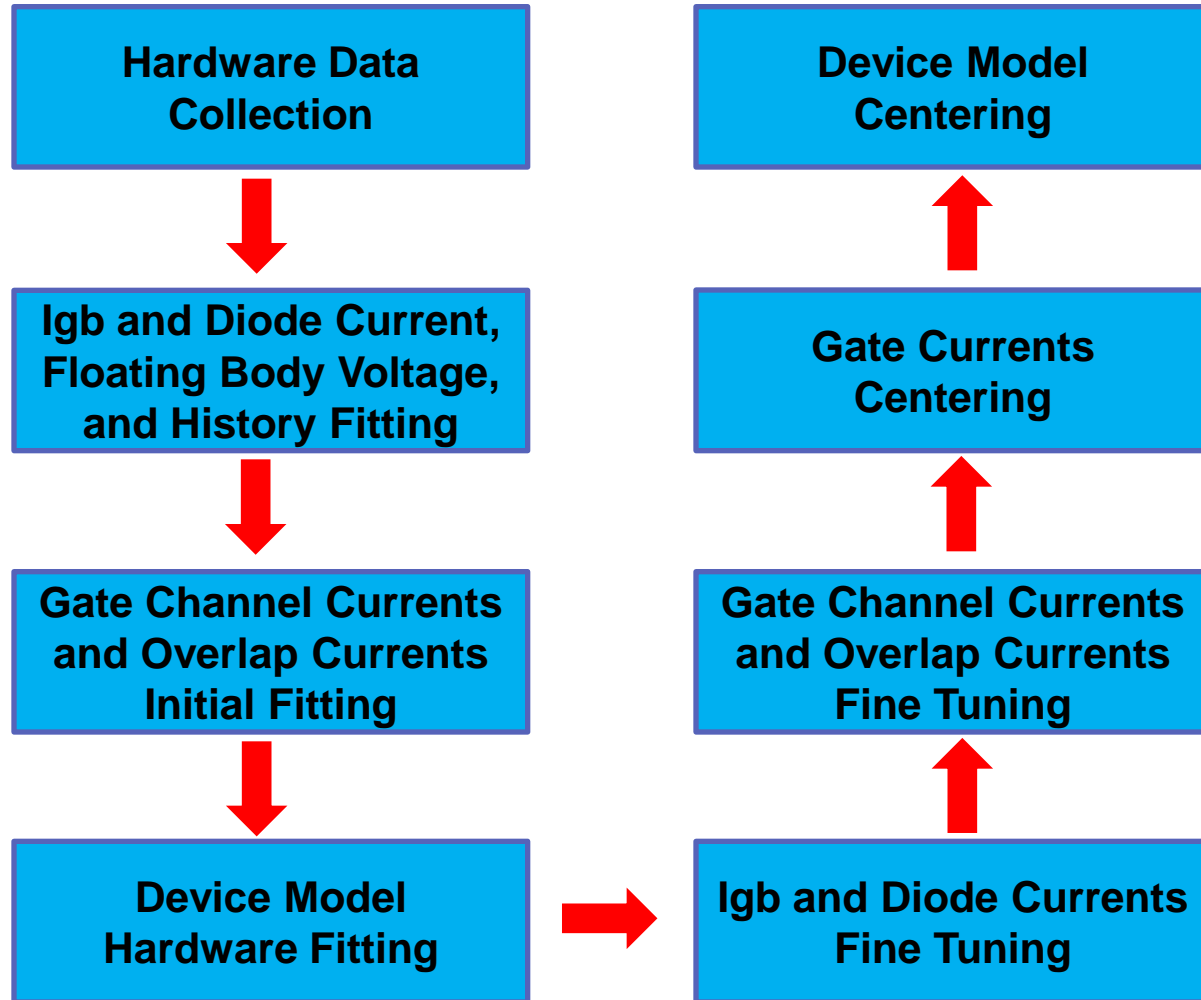


- High-K Metal Gate Technology**
- (a) allows increased scaling of the gate dielectric thickness.
 - (b) reduces polysilicon depletion.
 - (c) reduces leakage

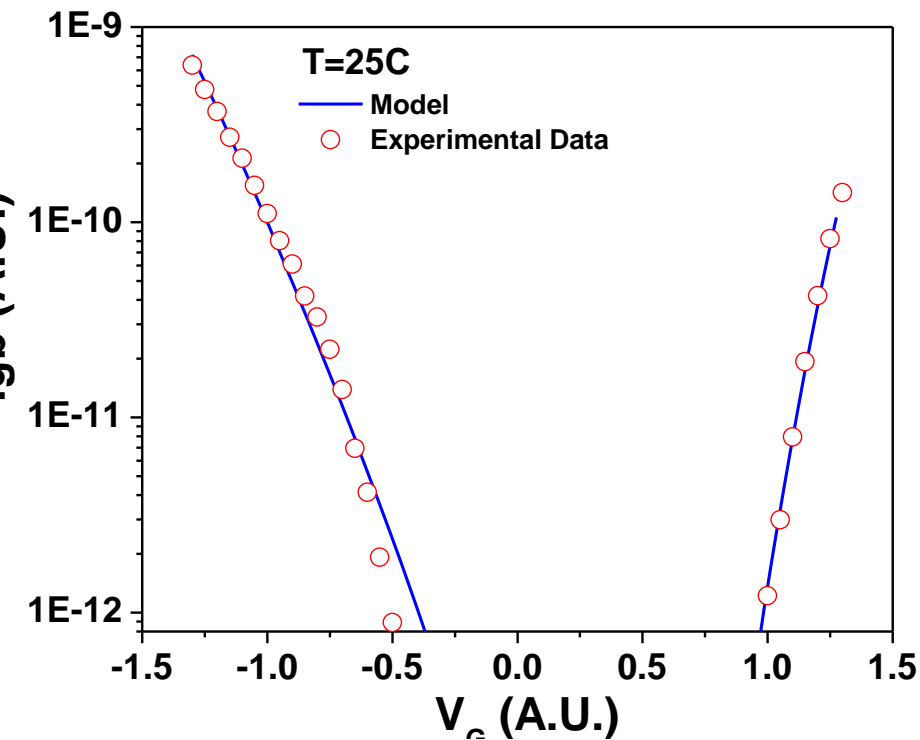


P. M. Zeitzoff, SST, p. 35, Feb, 2008

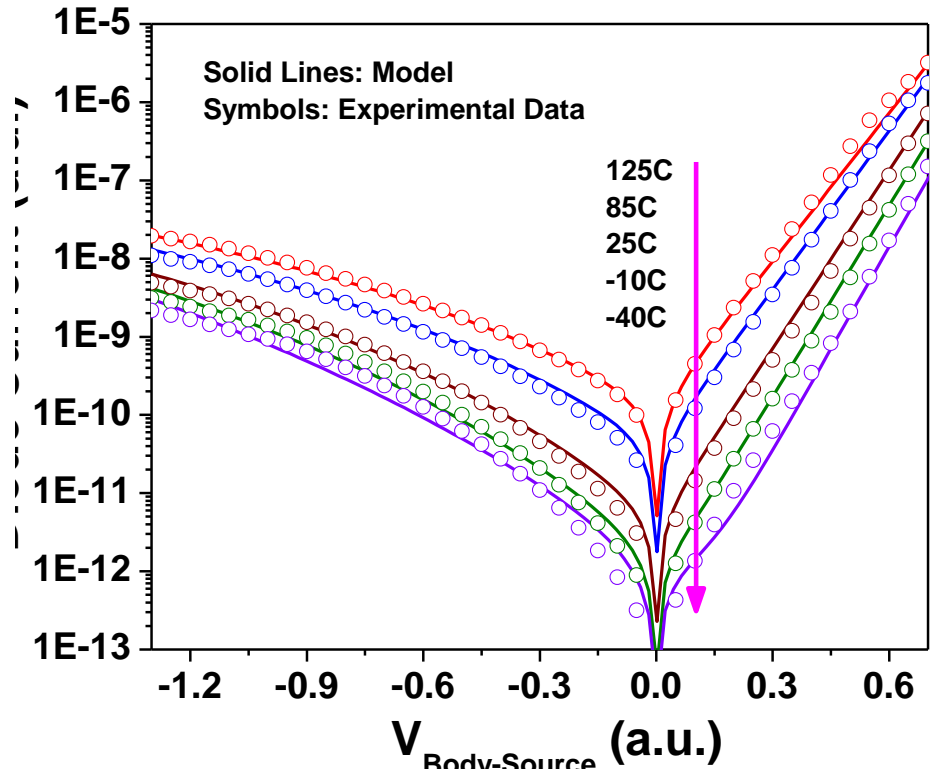
Gate Leakage Modeling Procedures



Experimental Data and Model Fit of I_{gb} and Diode Currents

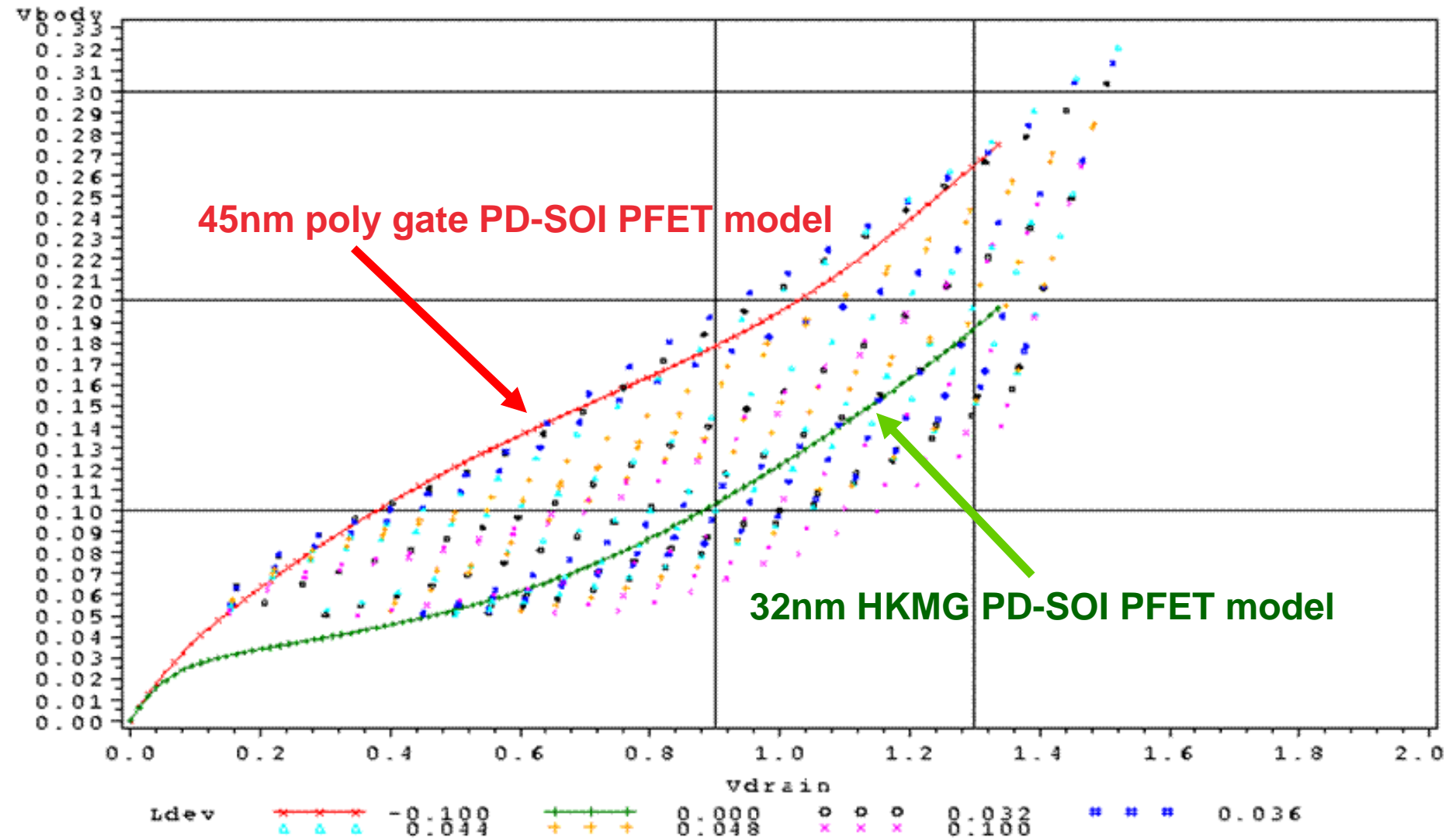


I_{gb} experimental data and model fit

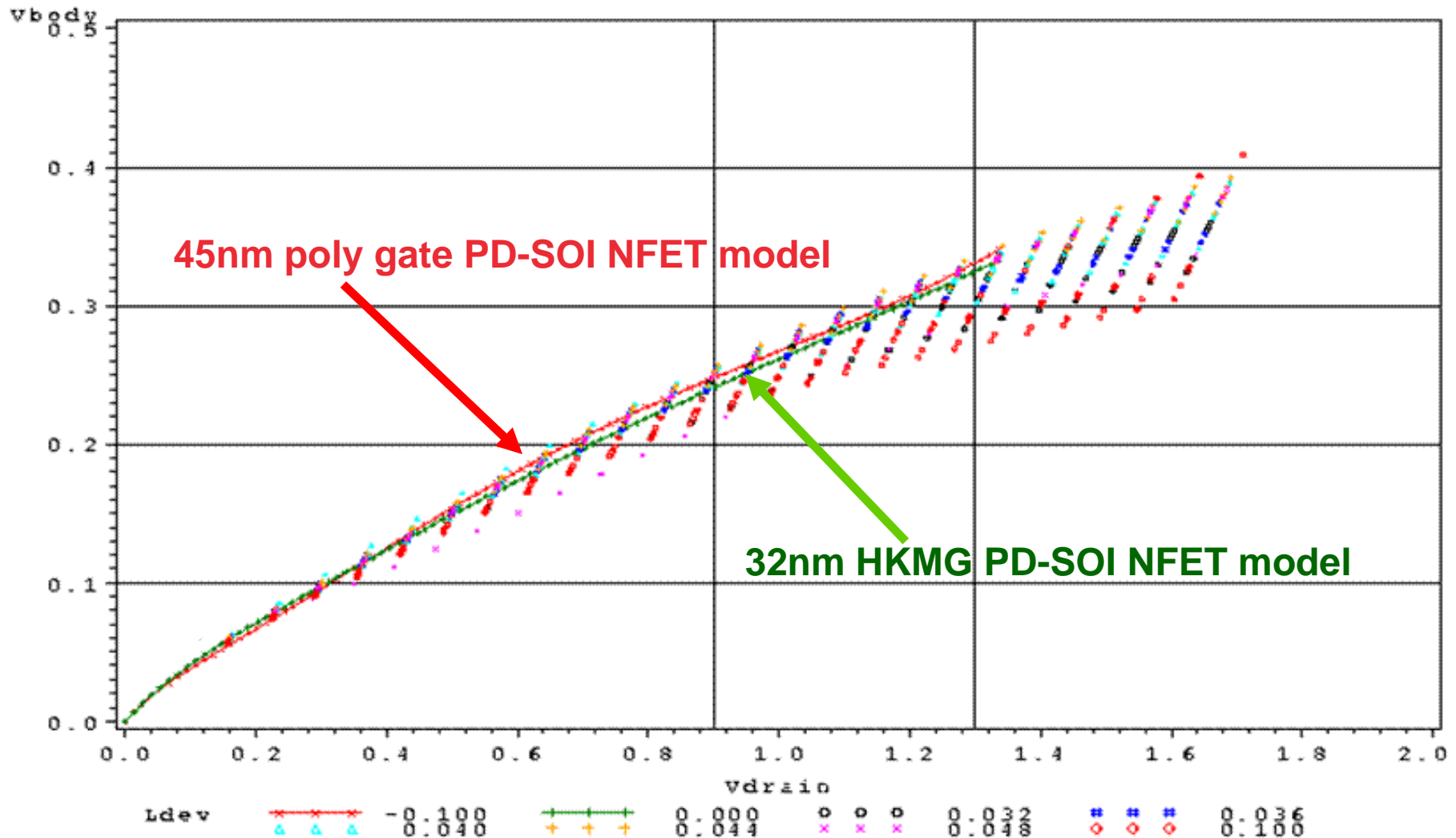


Diode current data and model fit

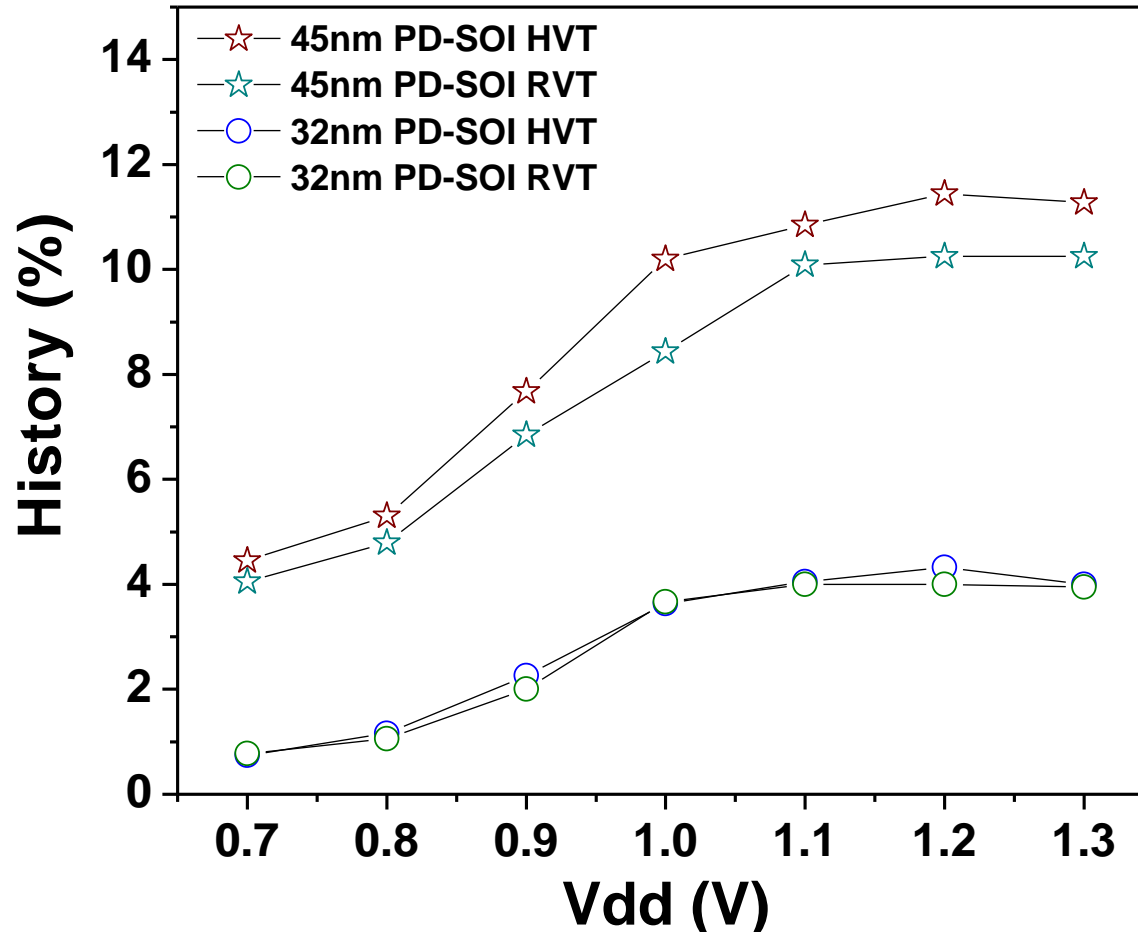
First Switching Floating Body Voltage of PD-SOI PFET at 85C



First Switching Floating Body Voltage of PD-SOI NFET at 85C

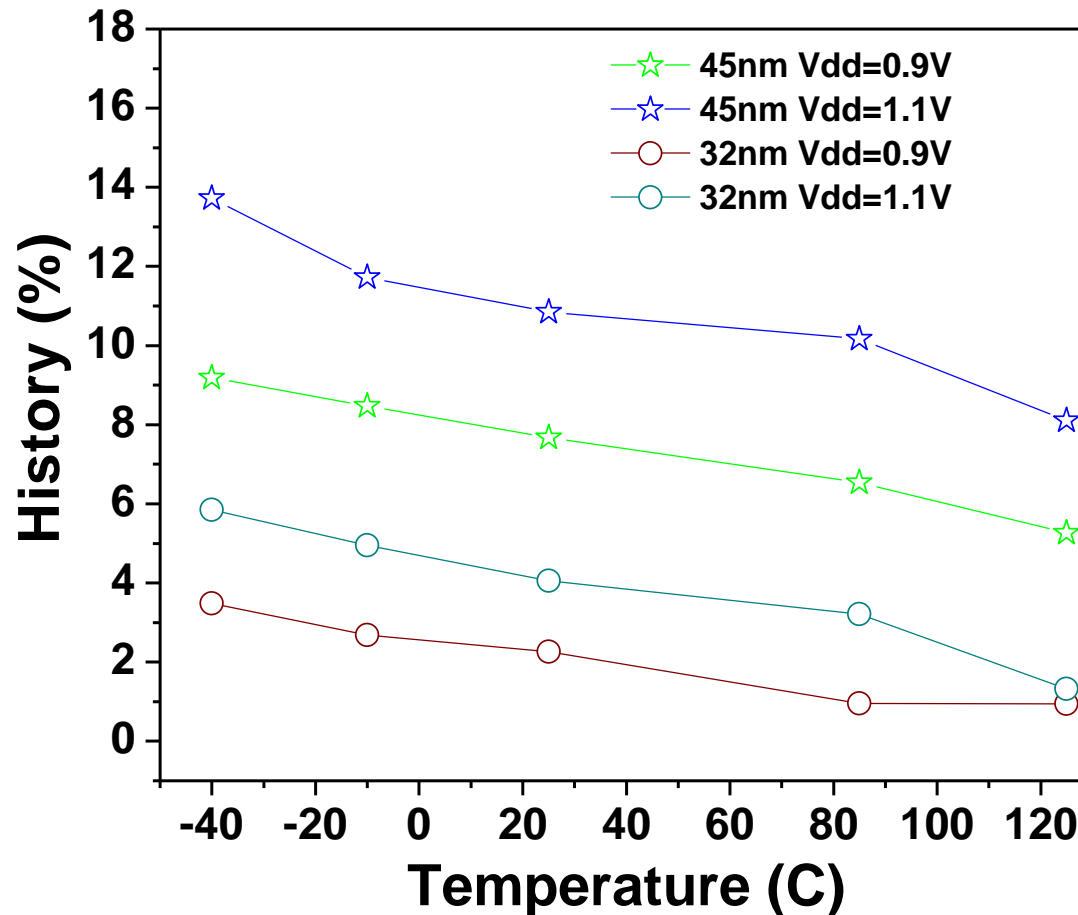


VDD Dependence of History Effect at 25C



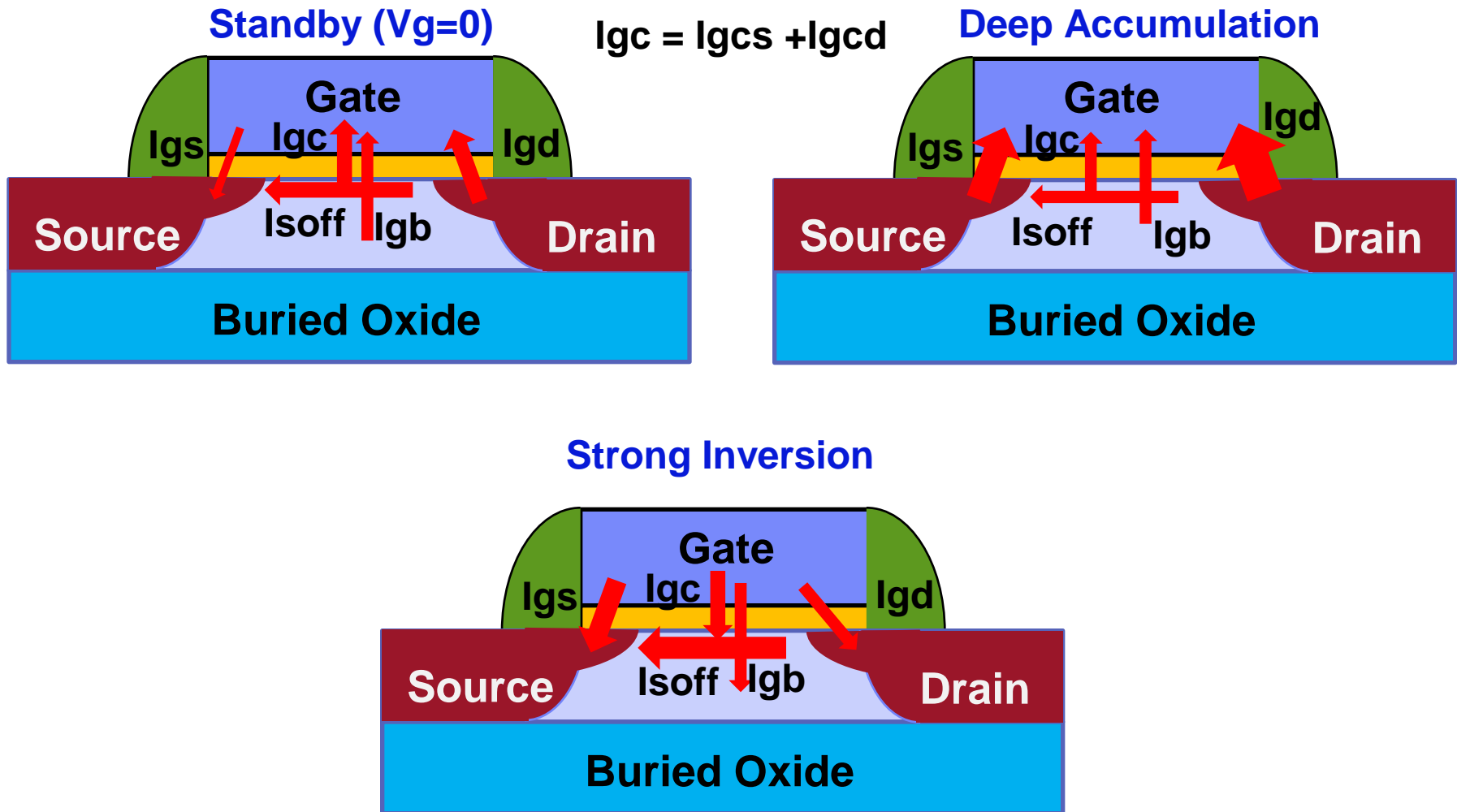
45nm Poly-Gate and 32nm HKMG PD-SOI RVT and HVT History Data

Temperature Dependence of History Effect



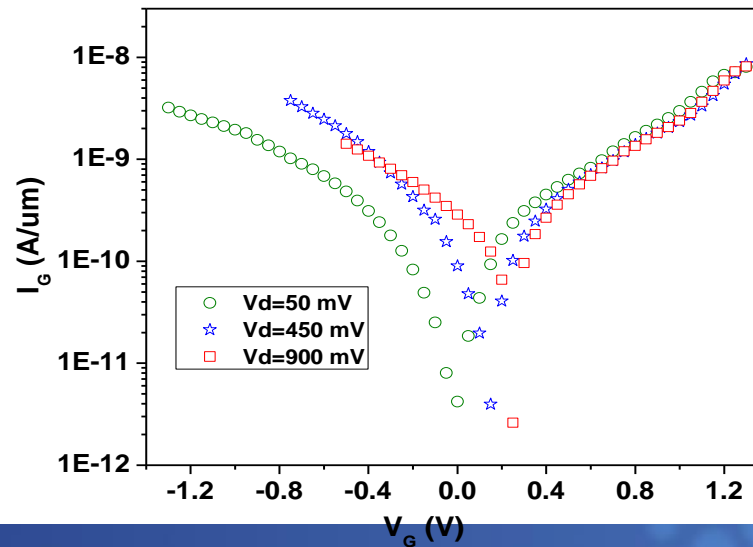
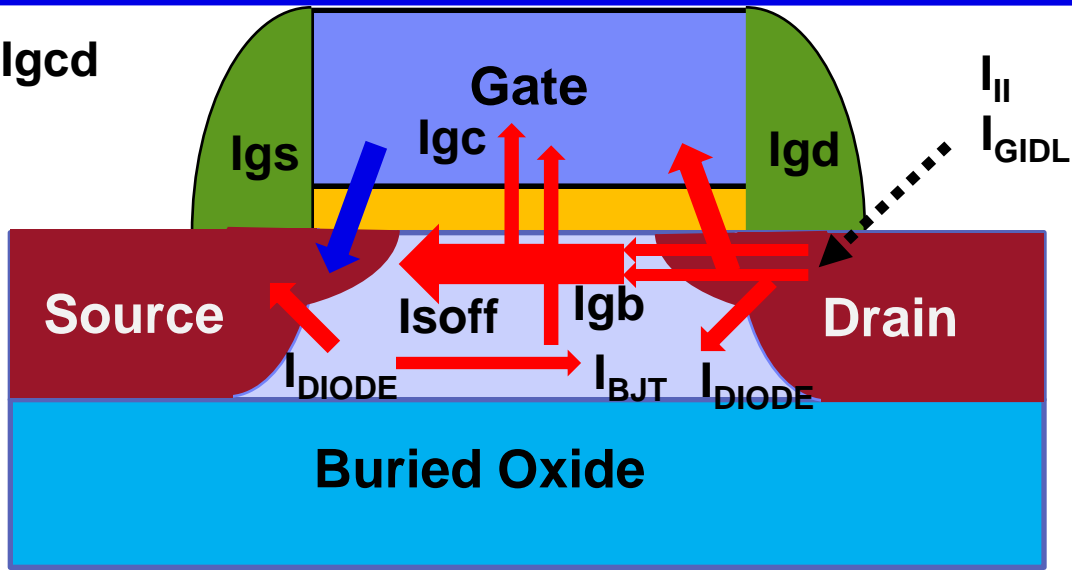
45nm Poly-Gate and 32nm HKMG PD-SOI HVT Temperature Dependence of History Effect

Gate Leakage Components

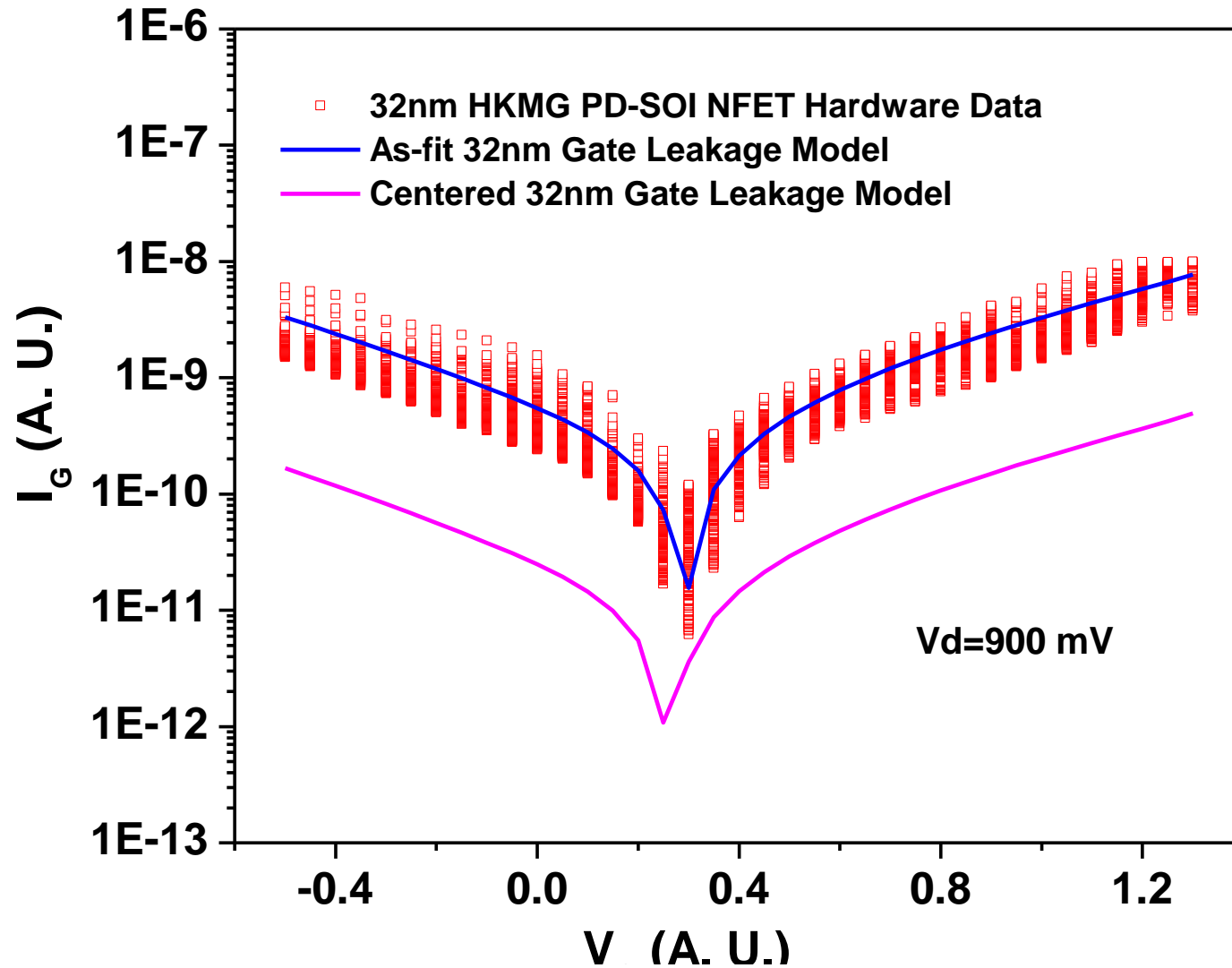


Sign Change of Gate Leakage

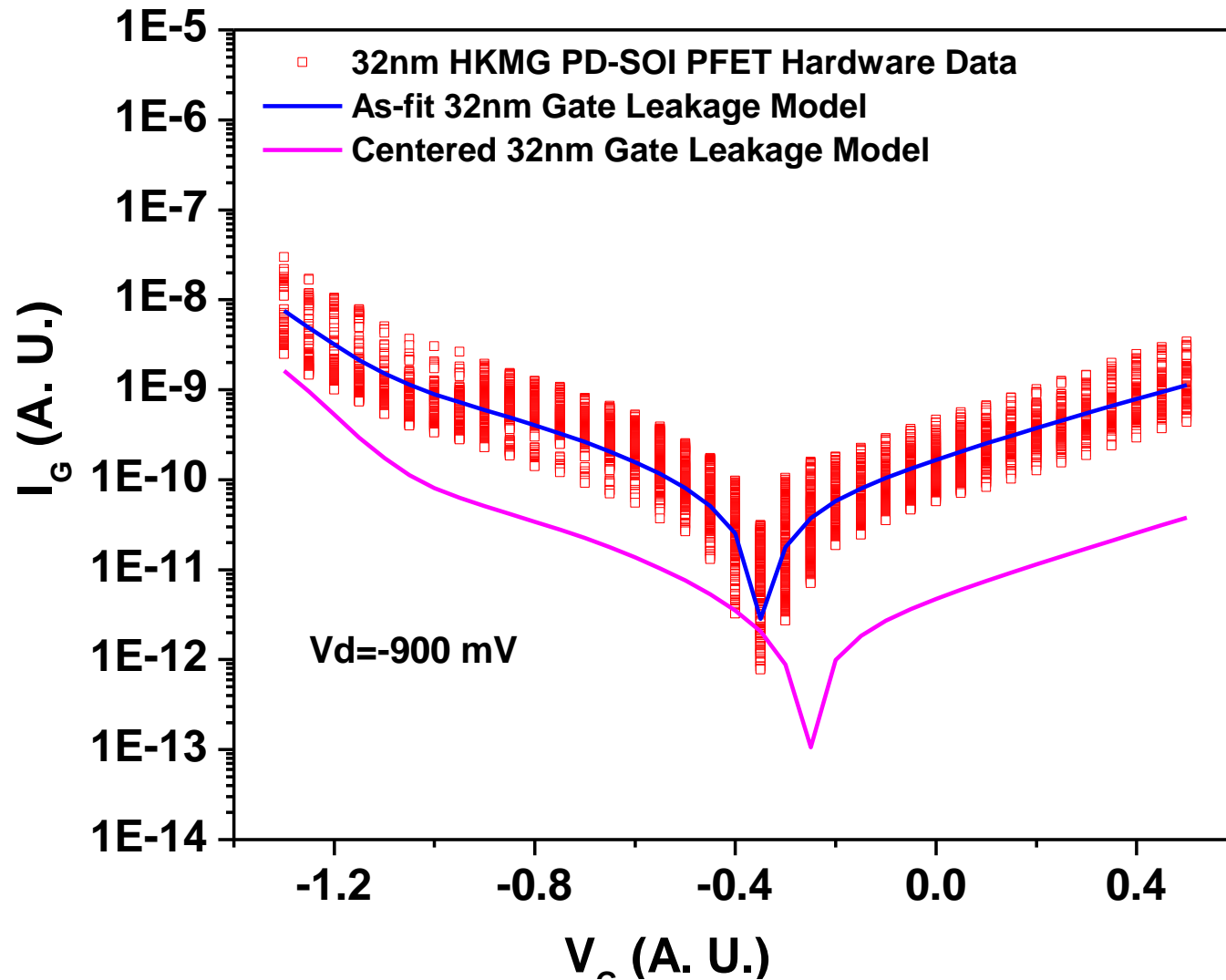
$$I_{gc} = I_{gcs} + I_{gcd}$$



NFET Gate Leakage Model and Hardware Correlation ($V_d=900$ mV)



PFET Gate Leakage Model and Hardware Correlation ($V_d = -900$ mV)



Summary

- ▣ **The gate leakage is largely reduced in 32nm HKMG PD-SOI transistors as compared to 45nm poly gate counterparts.**
- ▣ **The history in 32nm HKMG PD-SOI devices is significantly decreased compared to that of 45nm poly gate PD-SOI transistors.**
- ▣ **Comprehensive HKMG PD-SOI gate leakage and diode current models have been developed for 32nm HKMG PD-SOI circuit simulation and design.**

Acknowledgement

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