

# Impact of Gate-Induced-Drain- Leakage Current Modeling on Circuit Simulations in 45nm SOI Technology and Beyond

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# Outline

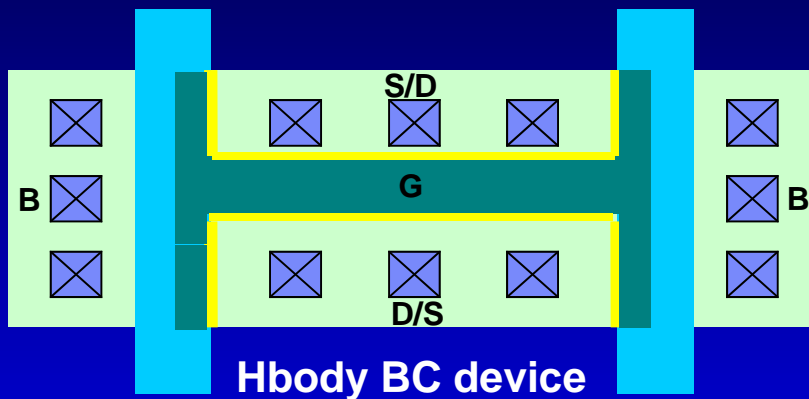
- ❑ Overview of GIDL modeling in SOI technologies
- ❑ GIDL current in 45nm PDSOI technology
- ❑ Model extraction and device simulation results
- ❑ Circuit simulation results
- ❑ Conclusion

# The Importance of GIDL Modeling

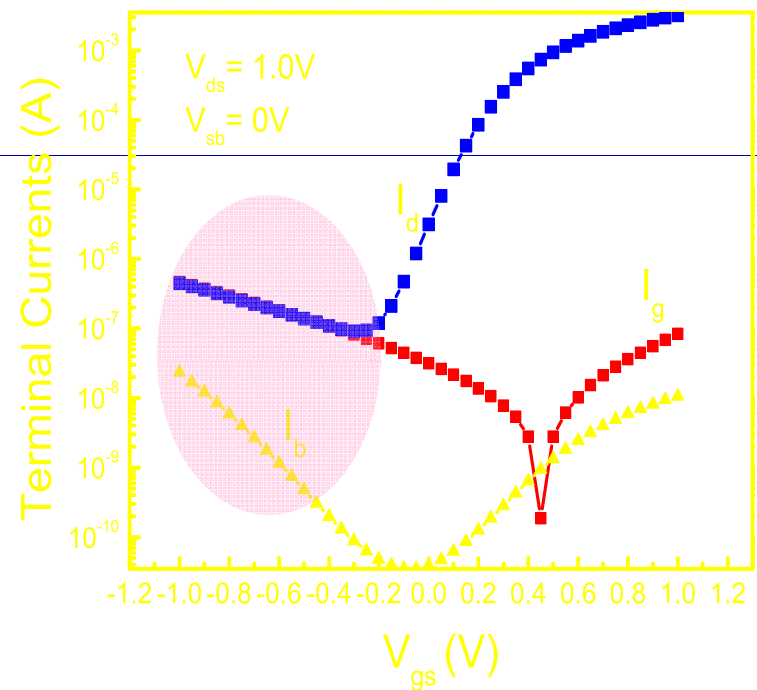


- ❑ In PDSOI devices, floating body potential is affected by the body currents
- ❑ GIDL will contribute to:
  - Leakage
  - Floating body effect
  - SOI history
  - Ring delay

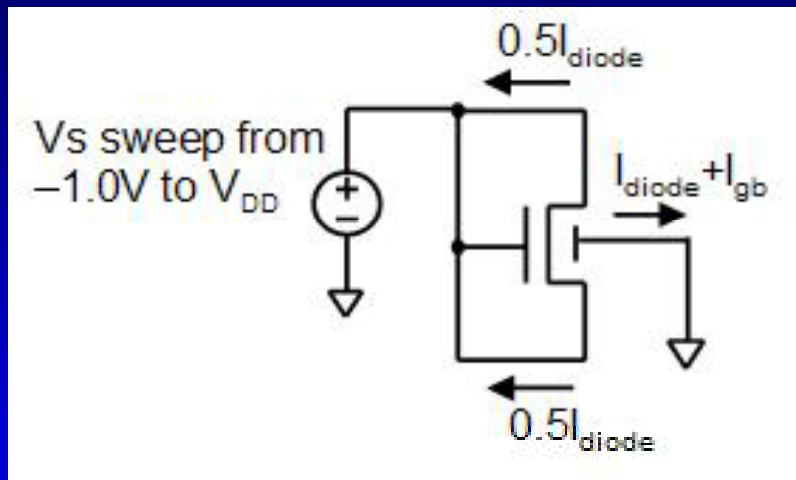
# Terminal Currents in 45nm SOI



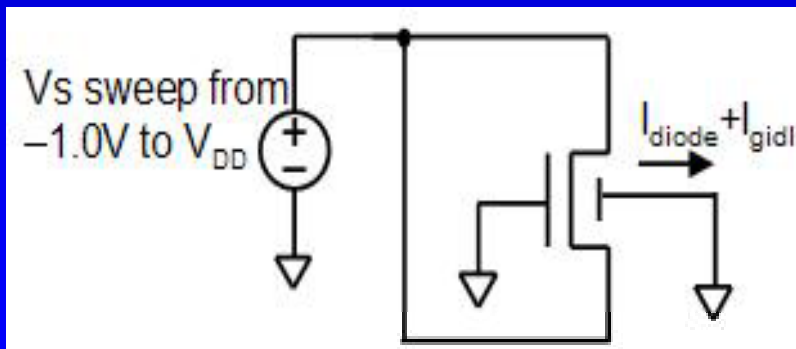
- ❑ Use Hbody BC device to measure body currents
- ❑ High gate leakage dominates drain current in accumulation region



# Measurement Setups for SOI GIDL Current Extraction

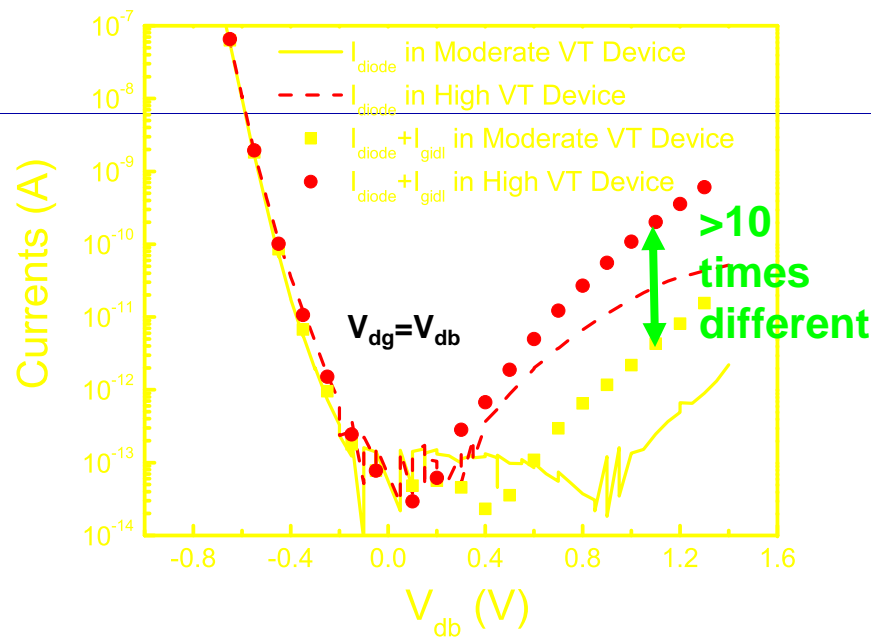


- Drain and source node are tied together and swept simultaneously with gate node from  $-1.0V$  to  $V_{dd}$ . Body node is grounded.



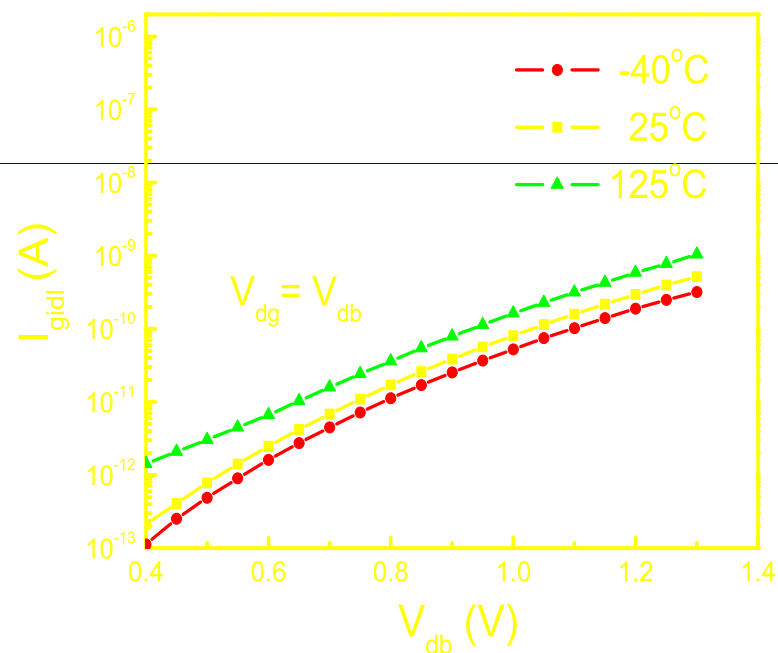
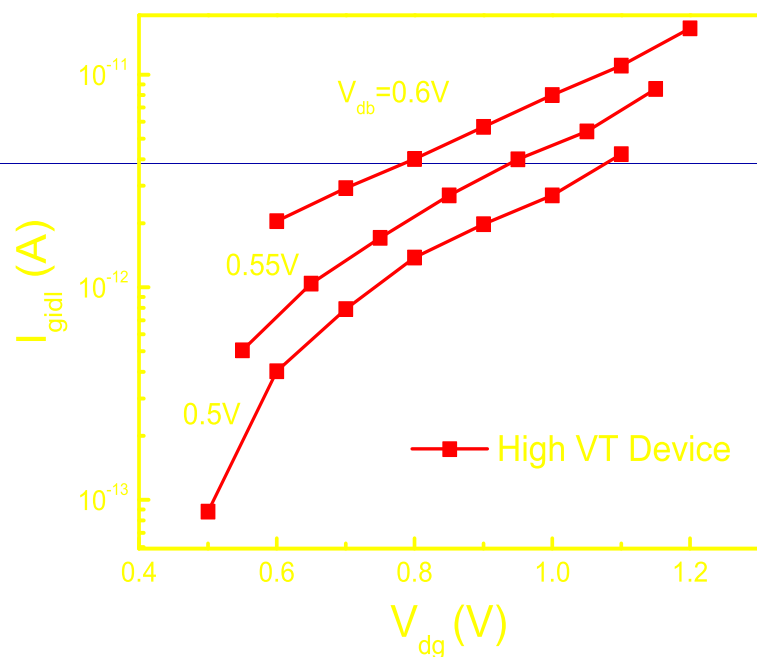
- Gate and body nodes are grounded. Drain and source node are tied together and swept simultaneously from  $-1.0V$  to  $V_{dd}$ .

# GIDL Current with Different Doping Concentration



- As channel doping concentration increases, GIDL current increases
- The B-S/B-D junction becomes more abrupt with higher channel doping, which enhances the transport of the current between drain and body

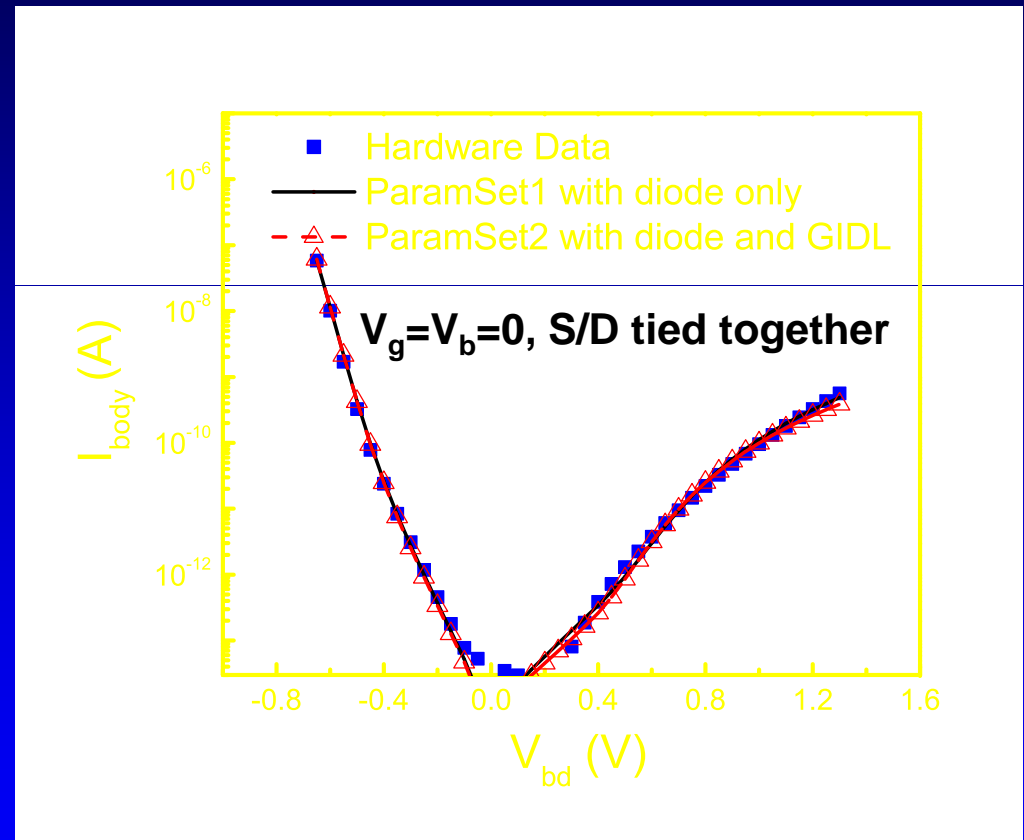
# GIDL Current Terminal Bias and Temperature Dependence



$$I_{GIDL} = \frac{A}{B} \cdot W \cdot (E^{\max})^2 \cdot \exp\left(-\frac{B}{E^{\max}}\right) \quad \text{where} \quad E^{\max} = \frac{\epsilon_{ox}}{\epsilon_{si}} \cdot \frac{V_{dg} - V_{fb} - \phi_s}{T_{ox}}$$

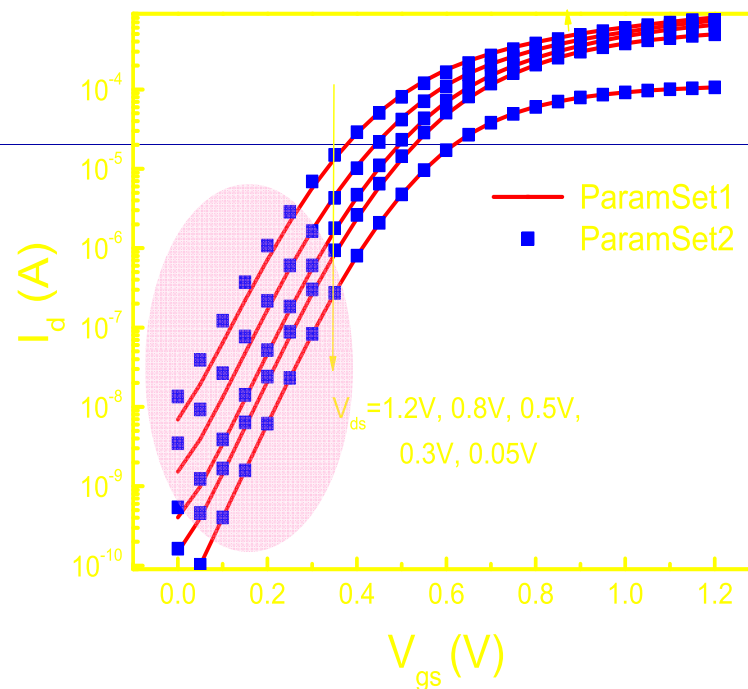
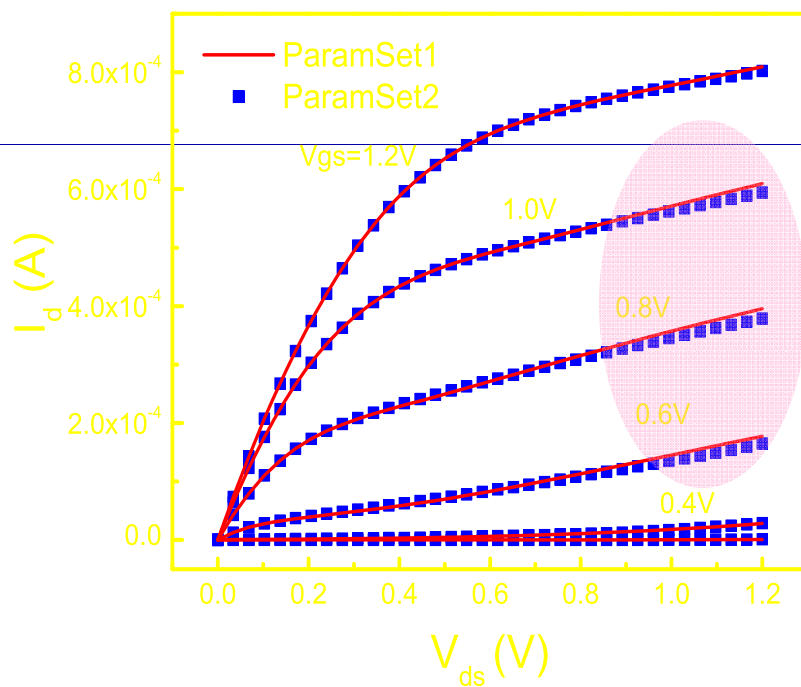
# Model Extraction

- $I_{\text{body}}$  data with  $V_{\text{gate}}=0$ ,  $V_{\text{source}}/V_{\text{drain}}$  sweep from -0.8 to 1.3V, 25C
- Diode and GIDL model parameters are different while keeping the rest of the model parameters the same



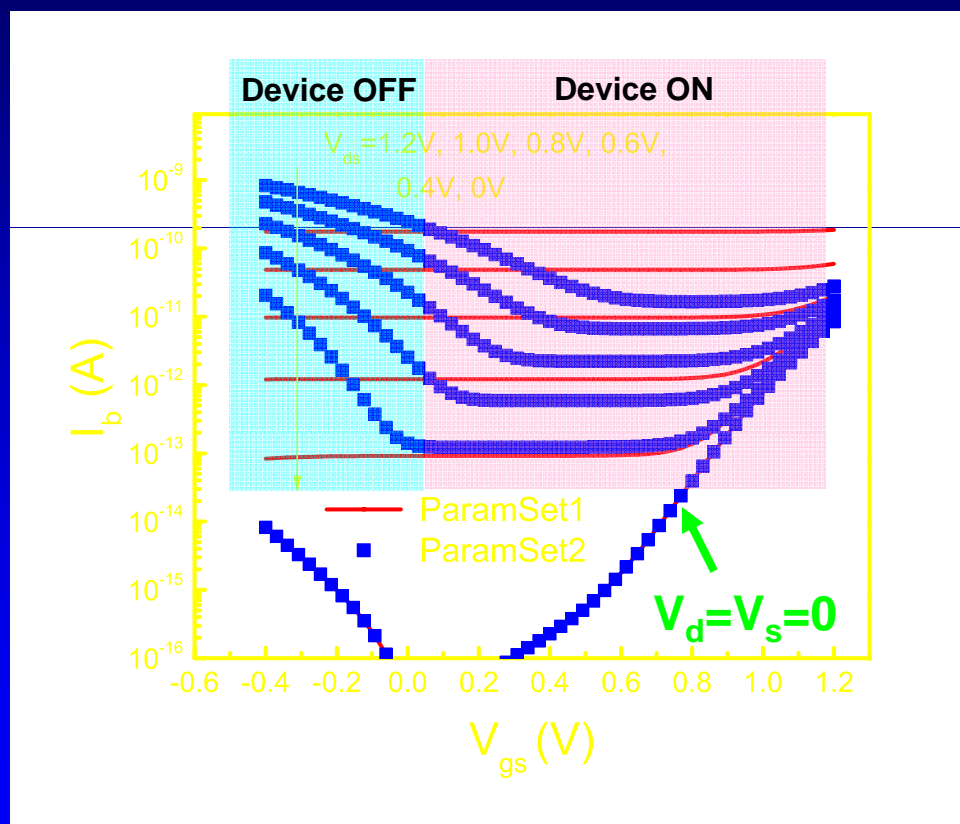
PFET,  $W_{\text{total}}=12 \mu\text{m}$ ,  $L=0.04 \mu\text{m}$

# Simulated Drain Currents using Different Models



PFET with  $W=1.0 \mu\text{m}$ ,  $L=0.04 \mu\text{m}$

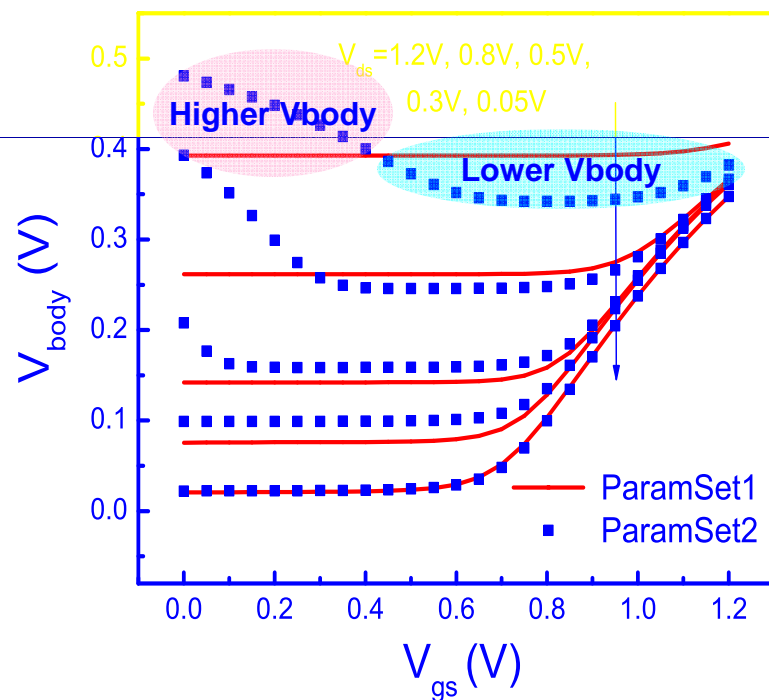
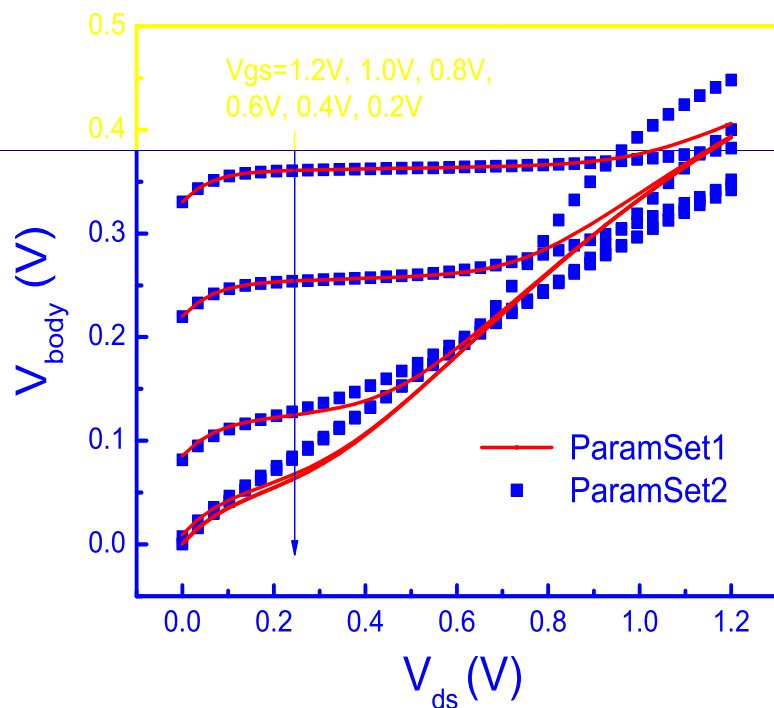
# Simulated Body Currents with Different Models



PFET with  $W=1.0 \mu\text{m}$ ,  $L=0.04 \mu\text{m}$

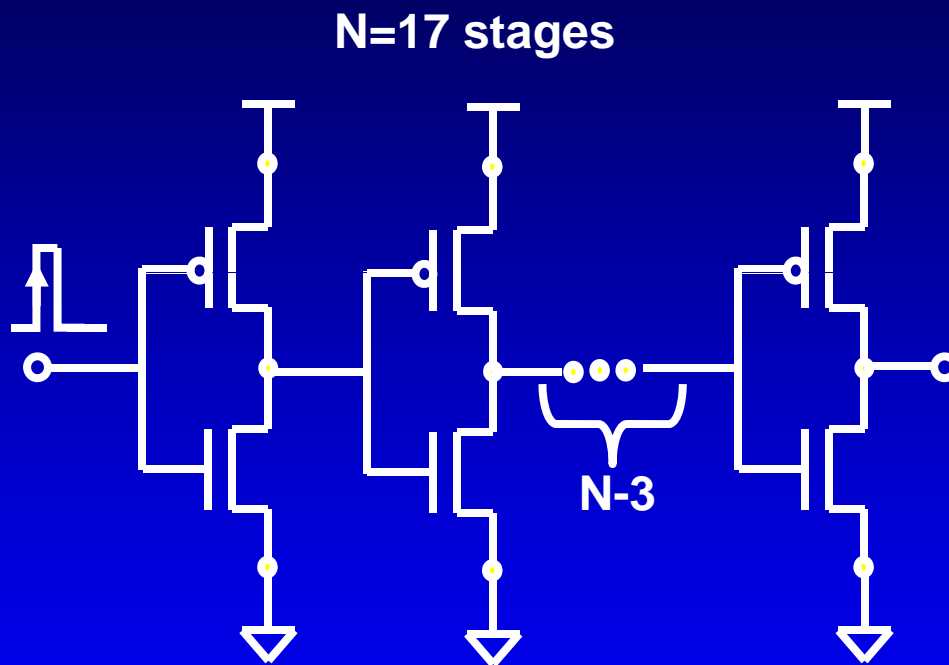
- ❑ At  $V_{ds}=0$ ,  $I_b$  is mainly  $I_{gb}$ , ParamSet1 and ParamSet2 produce same results
- ❑ ParamSet1 produces constant  $I_b$  in low  $V_{gs}$  region, while  $I_b$  is a function of both  $V_{ds}$  and  $V_{gs}$  with ParamSet2

# Simulated Floating Body Potential with Different Models



PFET with  $W=1.0 \mu m$ ,  $L=0.04 \mu m$

# Circuit Simulation Results



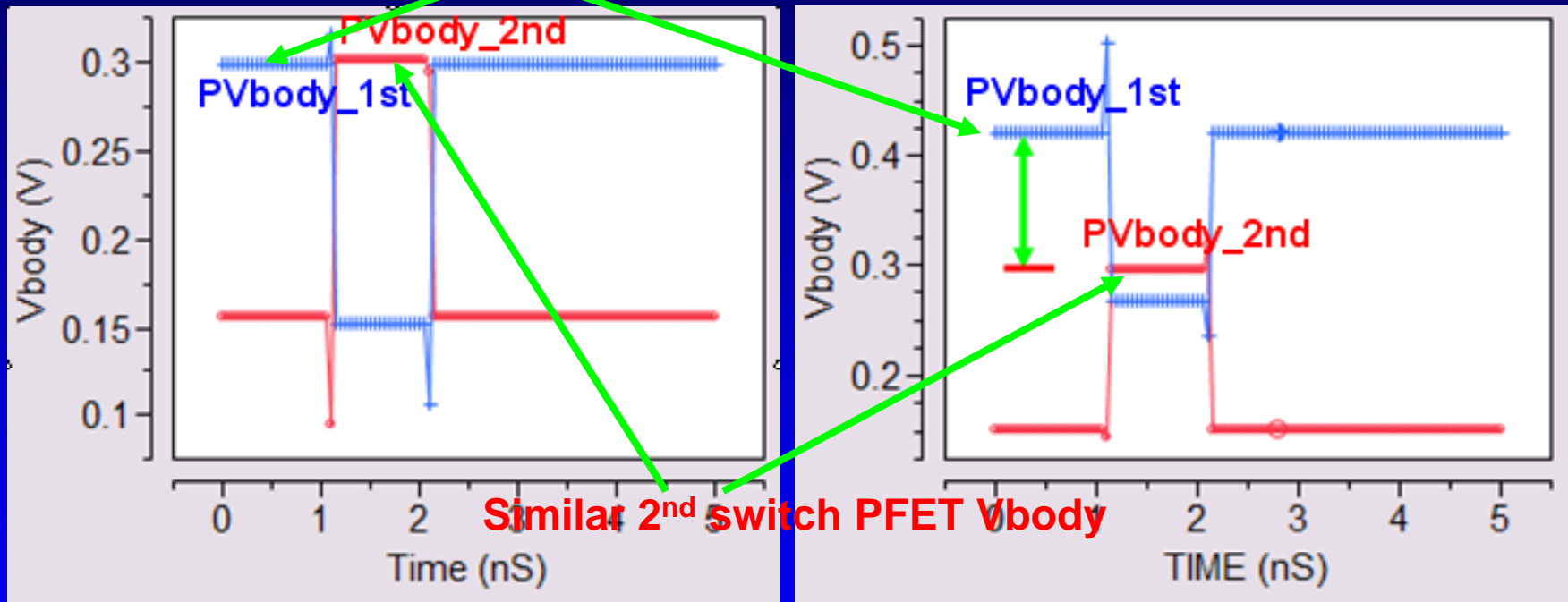
The inverter chain used in the simulation

- First switch delay (for PFET) is taken as the delay time of the even stages when the input first switches from high to low after a long idle time
- Second switch delay (for PFET) is taken as the delay time of the odd stages when the input switches the second time from high to low right after the first switch before the body discharges
- History

$$H = (\tau_{1st} - \tau_{2nd}) / \tau_{1st} \times 100\%$$

# PFET Floating Body Potential

Different 1<sup>st</sup> switch PFET Vbody



With ParamSet1

With ParamSet2

# Circuit Simulation Results

## □ Simulation Results

| PFET              | With diode only | With diode & gidl | Delta  |
|-------------------|-----------------|-------------------|--------|
| pullup Delay (ps) | 8.114           | 7.125             | -12.2% |
| pullup hist (%)   | 2.4             | -12.1             | -14.5  |
| vbody_1st (mV)    | 298             | 421               | 122    |
| vbody_2nd (mV)    | 302             | 296               | -6     |
| delta_vbody (mV)  | 4               | -124              | -128   |

Due to different floating body effect, average 1<sup>st</sup> switch pull-up delay is faster by more than 12%

Higher Vbody in 1<sup>st</sup> switch, mainly set by  $I_{gidl}$ ,  $I_{diode}$

Similar Vbody in 2<sup>nd</sup> switch, mainly set by forward  $I_{diode}$ , capacitive coupling, and  $I_{gb}$

# Conclusion

- ❑ Compared to a model without GIDL, floating body potential in a model with GIDL changes dramatically with gate biases
- ❑ Different GIDL modeling techniques significantly affect history and delay time in circuit simulations
- ❑ GIDL current needs to be accurately modeled even for digital circuit simulations

# Acknowledgement

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